

1 1. A method comprising:
2 receiving a data frame of a first size;
3 demultiplexing said data frame;
4 writing blocks of the demultiplexed data frame at
5 the first size into a register;
6 reading blocks of a second size, different from
7 said first size, from said register; and
8 multiplexing said blocks to form an output data
9 frame of the second size.

1 2. The method of claim 1 wherein receiving a data
2 frame of a first size includes receiving a 64-bit data
3 frame.

1 3. The method of claim 2 wherein demultiplexing said
2 data frame includes providing said data frame to a one to
3 thirty-three demultiplexer.

1 4. The method of claim 3 wherein writing blocks of
2 the demultiplexed data frame at the first size includes
3 writing blocks of 64-bits to a register.

1 5. The method of claim 4 wherein writing the blocks
2 into a register include writing 2,112 bits into a register.

1 6. The method of claim 5 including controlling a
2 write pointer at a frequency of approximately 161
3 MegaHertz.

1 7. The method of claim 5 wherein reading blocks of
2 the second size includes reading blocks of sixty-six bits
3 from said register.

1 8. The method of claim 7 including controlling a
2 read pointer at a frequency of approximately 156 MegaHertz.

1 9. The method of claim 7 wherein multiplexing said
2 blocks to form an output data frame of a second size
3 includes forming an output data frame by using a thirty-two
4 to one multiplexer.

1 10. The method of claim 1 including converting a
2 sixty-four bit data frame to a sixty-six bit data frame.

1 11. A device comprising:
2 a demultiplexer coupled to receive a data frame
3 of a first size;
4 a register coupled to receive data from said
5 demultiplexer; and

6 a multiplexer coupled to the output of said
7 register, the output of said multiplexer being a data frame
8 of a second size different from said first size.

1 12. The device of claim 11 including a first counter
2 to control the writing of data from said demultiplexer to
3 said register.

1 13. The device of claim 11 including a second counter
2 to control the reading of data from said register to said
3 multiplexer.

1 14. The device of claim 11 wherein data is written to
2 said register at approximately 161 MegaHertz and data is
3 read from said multiplexer at approximately 156 MegaHertz.

1 15. The device of claim 11 wherein said demultiplexer
2 receives a data frame of 64-bits and said multiplexer
3 outputs a data frame of 66-bits.

1 16. The device of claim 11 wherein said demultiplexer
2 is a one to thirty-three demultiplexer.

1 17. The device of claim 11 wherein said multiplexer
2 is a thirty-two to one multiplexer.

1 18. The device of claim 11 wherein said demultiplexer
2 writes data to said register in 64-bit blocks.

1 19. The device of claim 11 wherein said multiplexer
2 reads data from said register in 66-bit blocks.

1 20. The device of claim 11 wherein said demultiplexer
2 writes data in blocks of a first size to said register and
3 said multiplexer reads data in blocks of a second size,
4 different from said first size, from said register.

1 21. The device of claim 11 wherein said device is
2 part of a physical coding sublayer.

1 22. The device of claim 21 wherein said device is
2 part of a receiver in a fiber optic network.

1 23. A method comprising:
2 receiving a stream of data;
3 defining a window of a predetermined size within
4 said stream;
5 examining the window to determine whether at
6 least one synchronization bit is located within the data in
7 the window; and
8 shifting the window along said stream if a valid
9 synchronization bit is not found in the window.

1 24. The method of claim 23 including shifting the
2 window by a predetermined number of bits and filling the
3 opening created by shifting with a bit from a previous
4 cycle.

1 25. The method of claim 24 including storing bits
2 from each successive cycle and providing bits from previous
3 cycles to fill openings created by shifting in subsequent
4 cycles.

1 26. The method of claim 23 including successively
2 shifting said window by one bit along said stream of data
3 until valid synchronization bits are located.

1 27. The method of claim 23 including locating a pair
2 of synchronization bits in a 66-bit data frame.

1 28. The method of claim 23 including receiving a
2 block of data of said predetermined size in a multiplexer
3 and multiplexing said data into a register.

1 29. The method of claim 28 including applying two of
2 said bits from said register to an exclusive OR gate.

1 30. The method of claim 23 including providing 66-bit
2 blocks in successively shifted sets, each block shifted
3 one-bit relative to the other block, to a multiplexer and
4 successively applying said 66-bit blocks to a register.

1 31. The method of claim 23 including providing serial
2 data to a first array of multiplexers arranged in rows and
3 columns, wherein each row corresponds to a different window
4 position along the stream of data.

1 32. The method of claim 31 including writing the data
2 from a row of multiplexers in a first array to an array of
3 multiplexers in a second array.

1 33. A device comprising:
2 a first storage element to receive a stream of
3 data;
4 an element to define a window of a predetermined
5 size within said stream;
6 a detector to examine the window to determine
7 whether at least one synchronization bit is located within
8 the data in the window; and
9 a component to shift data along said stream into
10 said window if a valid synchronization bit is not found in
11 the window.

1 34. The device of claim 33 including:
2 a multiplexer coupled to said data stream and
3 said first storage element to receive data;
4 a second storage element coupled to the output of
5 said multiplexer to receive a data frame;
6 a gate coupled to said second storage element to
7 test for the presence of at least one synchronization bit
8 in said data frame in said second storage element; and
9 a control to determine whether or not valid
10 synchronization bits have been located in a series of data
11 frames.

1 35. The device of claim 34 wherein said control is a
2 state machine.

1 36. The device of claim 35 including a counter,
2 wherein said state machine controls the counter that
3 controls the operation of said multiplexer.

1 37. The device of claim 34 wherein said first and
2 second registers are sixty-six bit registers.

1 38. The device of claim 37 wherein said multiplexer
2 is a sixty-six to one multiplexer.

1 39. The device of claim 38 wherein said multiplexer
2 receives sixty-six shifts.

1 40. The device of claim 34 wherein said gate is an
2 exclusive OR gate.

1 41. The device of claim 40 wherein said exclusive OR
2 gate tests two bits of each data frame for the presence of
3 synchronization bits.

1 42. The device of claim 34 wherein said first storage
2 element stores bits from each successive cycle and provides
3 bits from previous cycles to fill openings created by
4 shifting in subsequent cycles.

1 43. The device of claim 42 including a counter that
2 receives a signal from said control and issues a signal to
3 said multiplexer to shift a window of data output by said
4 multiplexer along said serial data stream.

1 44. The device of claim 33 wherein said first storage
2 element includes an array of multiplexers arranged in rows
3 and columns.

1 45. The device of claim 44 wherein each row of
2 multiplexers provides one window of data.

1 46. The device of claim 45 including a second array
2 of multiplexers coupled to said first array of
3 multiplexers.

1 47. The device of claim 46 including a register that
2 receives the output from said second array of multiplexers.

1 48. The device of claim 47 including a gate to
2 determine whether or not at least one bit in said register
3 is a synchronization bit.

1 49. The device of claim 48 including a state machine
2 coupled to the output of said gate.

1 50. The device of claim 49 wherein said gate is an
2 exclusive OR gate.

1 51. The device of claim 49 including a state machine
2 coupled to the output of said gate.

1 52. The device of claim 51 including a counter
2 coupled to said state machine and said first array of
3 multiplexers to select a row of multiplexers in said first
4 array.

1 53. The device of claim 51 including a gear box to
2 convert 64-bit data frames to 66-bit data frames.

1 54. The device of claim 53 further including a
2 physical coding sublayer.

1 55. The device of claim 54 where said device is a
2 receiver for a fiber optic network.